

Publication Number: JP9-8460A

Date of publication of application: January 10, 1997

Application Number: JP7-151900

Date of filing: June 19, 1995

Applicant: IBIDEN Co., Ltd.

[Title Of The Invention]

ELECTRONIC COMPONENT MOUNTING BOARD

[Abstract]

PURPOSE: To provide an electronic component mounting board which can improve the efficiency of a wiring while the whole thickness of the board is prevented from being increased.

CONSTITUTION: A first group of pads are formed on the outermost layer of a build-up layer B1 formed by laminating alternately interlayer insulating layers 8a and 8b and internal layer conductor layers 9a and 9b. The layers 8a and 8b of the layer B1 consist of a photosensitive resin, which is hardly soluble to an acid or an oxidizing agent, and heat-resistant resin particles, which are soluble to the acid and the oxidizing agent. A wiring is always provided in the forward direction and centrifugally toward the outer peripheral parts of a board while the layer 9a linking the pads 12, which constitute the first group of the pads, with each other and an internal layer conductor layer 9a linking pads 13, which constitute a second group of the pads 13, with each other are respectively connected with the layers 8a and 8b and interlayer insulating layers 8a and 8b through via holes 11 formed in the layers 8a and 8b.

[Claim(s)]

[Claim 1] It comes to be formed in the outermost layer of a buildup layer which laminates a layer insulation layer and an inner layer conductor layer characterized by comprising the following by turns, A substrate for electronic-parts loading which it always comes to wire a forward direction and centrifugal toward a substrate peripheral part said inner layer conductor layer which connects said 1st contact button group and said 2nd contact button group being connected by viahole formed in said layer insulation layer.

The 1st contact button group that consists of two or more contact buttons formed in the state where it crowded in a center section by the side of the surface.

In a substrate for electronic-parts loading to which it electrically comes to connect the 2nd contact button group that consists of two or more contact buttons formed in a peripheral part by the side of a rear face, said 1st contact button group is a heat resistant resin particle of fusibility to acid, a photopolymer of poor solubility [oxidizer] and acid, or an oxidizer.

[Claim 2] The substrate for electronic-parts loading according to claim 1 characterized by comprising the following.

Resin and compound resin of thermoplastics in which said layer insulation layer is poorly soluble, and sensitization-ized thermosetting resin to acid or an oxidizer.

A heat resistant resin particle of the fusibility of acid or an oxidizer.

[Claim 3] Resin which is poorly soluble and sensitization-ized thermosetting resin to said acid or an oxidizer, Are any at least one resin chosen from epoxy acrylate and photosensitive polyimide, and said thermoplastics, The substrate for electronic-parts loading according to claim 2 which is any at least one resin chosen from among polyether sulphone, polysulfone, phenoxy resin, and polyethylene.

[Claim 4]The substrate for electronic-parts loading according to claim 2 or 3 which is any at least one as which said heat resistant resin particle is chosen from among an amino resin particle and an epoxy resin particle.

[Detailed Description of the Invention]

[0001]

[Industrial Application]This invention relates to the substrate for electronic-parts loading.

[0002]

[Description of the Prior Art]Conventionally, bare chips, such as a flip chip, and the substrate 21 for electronic-parts loading as shown, for example in drawing 3 as a printed wired board for carrying packages, such as BGA, are known.

[0003]The double-sided board which has the conductor layer mainly formed by the subtractive process in a rear surface as the base board 22 is used for this kind of substrate 21 for electronic-parts loading. The area for element placements is established in the center section of the surface of the base board 22. In the area, after the 1st pad group that consists of many pads 23 has crowded, it is formed. The formation position of each of said pad 23 supports the position of the vamp BP in the bottom of the bare chip C1 which is electronic parts. On the other hand, the 2nd pad group that consists of many pads 24 is formed in the peripheral part of the rear face of the base board 22. On these pads 24, the vamp 25 is formed as a projection electrode for aiming at connection by the side of a mother board. The through hole 26 of a large number which penetrate a rear surface is formed in the peripheral part of the base board 22. These through holes 26 and the pad 23 by the side of the surface are connected via the conductive pattern 27 formed in the surface of the base board 22. The through hole 26 and the pad 24 by the side of a rear face are connected via the conductive pattern 28 similarly formed in the rear face of the base board 22. As a result, in this substrate 21 for electronic-parts loading, it is in the state where the 1st pad group and 2nd pad group were electrically connected mutually.

[0004]

[Problem(s) to be Solved by the Invention]However, when it is the conventional substrate 21 for electronic-parts loading, as shown in drawing 3, it has the structure of pulling back again the wiring once pulled out to the peripheral part to the surface side to a central direction at the rear-face side. Therefore, the wiring which connects between the pads 23 and 24 became long more than needed easily, and wiring efficiency was bad. In the electronic component mount device using such a substrate 21 for electronic-parts loading, there was a problem that achievement of improvement in the speed was difficult.

[0005]In order to connect between the pads 23 and 24 by the shortest wire length, it is thought that what is necessary is just to form the through hole 26 in the substrate center section instead of a substrate peripheral part. However, the space (dead space) which only the forming face integration of the through hole 26 cannot wire in this case will be made. Therefore, when it was going to secure the space which can wire, there was a situation that the whole enlargement was not avoided.

[0006]It is made in order that this invention may solve the above-mentioned technical problem, and the purpose is in providing the substrate for electronic-parts loading which can raise wiring efficiency, avoiding the whole enlargement.

[0007]

[Means for Solving the Problem]In order to solve the above-mentioned technical problem,

the invention according to claim 1, In a substrate for electronic-parts loading to which it electrically comes to connect the 1st contact button group that consists of two or more contact buttons formed in the state where it crowded in a center section by the side of the surface, and the 2nd contact button group that consists of two or more contact buttons formed in a peripheral part by the side of a rear face, It comes to form said 1st contact button group in the outermost layer of a buildup layer which laminates by turns a layer insulation layer and an inner layer conductor layer which become a poorly soluble photopolymer, acid, or an oxidizer from a heat resistant resin particle of fusibility to acid or an oxidizer, Said inner layer conductor layer which connects said 1st contact button group and said 2nd contact button group makes the gist a substrate for electronic-parts loading which it always comes to wire a forward direction and centrifugal toward a substrate peripheral part, being connected by viahole formed in said layer insulation layer.

[0008]The invention according to claim 2 makes it the gist for said layer insulation layer to consist of resin and compound resin of thermoplastics which are poorly soluble and sensitization-ized thermosetting resin to acid or an oxidizer, and a heat resistant resin particle of the fusibility of acid or an oxidizer in claim 1.

[0009]Resin in which the invention according to claim 3 is poorly soluble, and sensitization-ized thermosetting resin to said acid or an oxidizer in claim 2, Are any at least one resin chosen from epoxy acrylate and photosensitive polyimide, and said thermoplastics, Let it be the gist to be any at least one resin chosen from among polyether sulphone, polysulfone, phenoxy resin, and polyethylene.

[0010]The invention according to claim 4 makes it the gist for said heat resistant resin particle to be any at least one chosen from among an amino resin particle and an epoxy resin particle in claim 2 or 3.

[0011]

[Function]According to the invention according to claim 1 to 4, the length of the wiring to which only the part which does not pull back wiring connects between the 1st and 2nd contact buttons becomes short. Since the heat resistant resin particle is contained in the layer insulation layer, dispersion of light takes place easily at the time of exposure. Therefore, even if it is a high viahole of an aspect ratio, it becomes difficult to produce the development remainder at the time of the formation. Therefore, the viahole of a byway can be formed easily and certainly. So, since a viahole can be formed in the center section in which wiring crowds, wiring can be arranged from a center section to a forward direction to a peripheral part via this viahole, and the wire length between the 1st and 2nd contact buttons becomes short only the part which does not pull back wiring.

[0012]

[Example]Hereafter, one example which materialized this invention is described in detail based on drawing 1. In this substrate 1 for electronic-parts loading, the double-sided board 2 is used as a base board. This double-sided board 2 has the conductor layers 3 and 4 formed by the subtractive process at both the surface S1 of the substrate 5 made of resin, and the rear face S2. It migrates to the whole surface and the through hole 6 for aiming at the flow between the conductor layers 3 and 4 is formed in this double-sided board 2. It fills up with the conductive resin 7 grade containing metal powder, such as copper, in these through holes 6.

[0013]The buildup layer B1 which laminates the layer insulation layers 8a and 8b and the conductor layers 9a and 9b by turns, and B-2 are formed in the surface S1 and the rear face

S2 of the double-sided board 2 which is a base board, respectively.

[0014]Surface S1 The permanent resist 10 is formed in the upper surface of the 1st layer insulation layer 8a located in a inner layer in the buildup layer B1 formed in the side. The inner layer conductor layer 9a is formed in the portion in which this permanent resist 10 is not formed. And this inner layer conductor layer 9a and the inner layer conductor layer 3 by the side of the double-sided board 2 are electrically connected by the viahole 11 provided in the 1st layer insulation layer 8a. The permanent resist 10 is similarly formed on the 2nd layer insulation layer 8b provided in said layer insulation layer 8a. The outer layer conductor layer 9b is formed in the portion in which this permanent resist 10 is not formed. And this outer layer conductor layer 9b and inner layer conductor layer 9a are electrically connected by the viahole 11 provided in the 2nd layer insulation layer 8b. The center section of the 2nd layer insulation layer 8b is the element-placement area for carrying the bare chip C1 of LSI as electronic parts. In this area, after the 1st pad group that consists of many pads 12 as a contact button has crowded, it is formed. The position of these pads 12 supports the formation position of the vamp BP formed in the bottom of the bare chip C1.

[0015]Surface S2 In buildup layer B-2 formed in the side, the permanent resist 10 is formed on the 1st layer insulation layer 8a located in a inner layer. The inner layer conductor layer 9a is formed in the portion in which this permanent resist 10 is not formed. And this inner layer conductor layer 9a and the inner layer conductor layer 4 by the side of the double-sided board 2 are electrically connected by the viahole 11 provided in the 1st layer insulation layer 8a. The permanent resist 10 is similarly formed on the 2nd layer insulation layer 8b provided in said layer insulation layer 8a. The outer layer conductor layer 9b is formed in the portion in which this permanent resist 10 is not formed. And this outer layer conductor layer 9b and inner layer conductor layer 9a are electrically connected by the viahole 11 provided in the 2nd layer insulation layer 8b. The 2nd pad group that consists of many pads 13 as a contact button is formed in the peripheral part of the 2nd layer insulation layer 8b. On these pads 13, the vamp 14 is formed as a projection electrode for aiming at electric connection by the side of the mother board which is not illustrated.

[0016]In this substrate 1 for electronic-parts loading, the pad 12 which constitutes the 1st pad group is connected to the through hole 6 via the outer layer conductor layer 9b, the viahole 11, the inner layer conductor layer 9a, the viahole 11, and the inner layer conductor layer 3. And the inner layer conductor layer 4 connected to the through hole 6 is connected to the pad 13 which constitutes the 2nd pad group via the viahole 11, the inner layer conductor layer 9a, the viahole 11, and the outer layer conductor layer 9b. The inner layer conductor layers 3, 4, and 9a and the outer layer conductor layer 9b are always wired a forward direction and centrifugal toward the substrate peripheral part, being connected by the viahole 11. About some things of said pads 12 and 13, it may be direct connected to the upper surface of the viahole 11, without being connected to the outer layer conductor layer 9b. The viahole 11 in the 1st layer insulation layer 8a and the viahole 11 in the 2nd layer insulation layer 8b may be arranged in series.

[0017]Here, the buildup layer B1 and the layer insulation layers 8a and 8b which constitute B-2 need to become a photopolymer, and poorly soluble acid or oxidizer from the heat resistant resin particle of fusibility to acid or an oxidizer. This is because dispersion of light takes place easily at the time of exposure, and it will therefore become

difficult to produce the development remainder at the time of the formation even if it is the high viahole 11 of an aspect ratio if the heat resistant resin particle is contained. When a mere photopolymer is used, it becomes difficult to form the viahole 11 of a byway (about 80 micrometers or less in diameter).

[0018]As for said layer insulation layers 8a and 8b, it is preferred to consist of resin and compound resin of thermoplastics which are poorly soluble and sensitization-ized thermosetting resin to acid or an oxidizer, and a heat resistant resin particle of the fusibility of acid or an oxidizer. The reason is for forming the anchor for raising the adhesion of the agent between layers, and copper plating. Acid here or oxidizer refers to chromic acid, chromate salt, fault manganese salt, etc. which are used, for example in a surface roughening process.

[0019]As for the resin which is poorly soluble and sensitization-ized thermosetting resin to said acid or an oxidizer, it is preferred that it is any at least one resin chosen from epoxy acrylate and photosensitive polyimide (photosensitive PI). This is because it has high heat resistance and high intensity.

[0020]As for said thermoplastics, it is preferred that it is any at least one resin chosen from among polyether sulphone (PES), polysulfone (PSF), phenoxy resin, and polyethylene (PE). The reason is because high Tg and the rate of high elasticity can be given with the characteristic of said thermosetting resin held.

[0021]As for said heat resistant resin particle, it is preferred that it is any at least one chosen from among an amino resin particle and epoxy resin (EP resin) particles. The reason is not degrading the characteristic of a layer insulation layer. Since the epoxy resin hardened with the amine system hardening agent has hydronalium EKISHI ether structure, especially the particles that consist of this resin have the advantageous character to be easy to melt. As an amino resin particle, it is selectable in melamine resin, urea resin, guanamine resin, etc., for example. Especially, it is preferred to choose melamine resin in the point that an electrical property, PCT, and the HHBT characteristic become good.

[0022]As for the particle diameter of said heat resistant resin particle, it is good that it is 10 micrometers or less. This is because interlayer film thickness can be made thin and formation of a fine pattern can be performed. As shape of a heat resistant resin particle, various things, such as the shape of a real ball, a spall, and floc, can be chosen.

[0023]Such a substrate 1 for electronic-parts loading of composition is producible by passing through the following procedures, for example. The preparing method of the adhesives for additives for forming the layer insulation layers 8a and 8b is as follows. Oligomer of the photosensitive grant which acrylic-ized 25% of the epoxy groups of cresol novolak type epoxy resin (CNA25, molecular weight 4000), PES (molecular weight 17000), an imidazole hardening agent (made in Shikoku Chemicals, trade name:2B4 MZ-CN), it is a photosensitive monomer -- (TMPTA) and, [trimethyl doria] It mixes using DMF using a photoinitiator (the Ciba-Geigy make, trade name:I-907) by the following presentation, Furthermore, a thing with a mean particle diameter of 5.5 micrometers to this mixture for epoxy resin powder (the Toray Industries make, a trade name: TOREPARU EP-B) 20 weight sections, It is considered as the adhesives for additives by adjusting and kneading a thing with a mean particle diameter of 0.5 micrometer to the viscosity of 120 cps with 3 rolls continuously a HOMODI spar agitator, after mixing ten weight sections. Subsequently, after applying these adhesives to whole both sides of the double-sided board 2, it dries at 80 ** and UV curing and heat curing are performed further. As a result, the 1st

layer insulation layer 8a is formed first.

[0024]Next, a roughened surface provided with many crevices for anchors is formed by processing the surface of this 1st layer insulation layer 8a by roughening agents, such as chromic acid. Then, the inner layer conductor layer 9a and the viahole 11 are formed by performing catalyst core grant, formation of the permanent resist 10, activation, and non-electrolytic copper plating in accordance with a conventional method.

[0025]The 2nd layer insulation layer 8b is formed by applying and hardening the same adhesives for additives to both sides. Subsequently, a roughened surface is formed by processing the surface of the 2nd obtained layer insulation layer 8b by a roughening agent. Then, catalyst core grant, formation of the permanent resist 10, activation, and non-electrolytic copper plating are performed, and the outer layer conductor layer 9b, the pads 12 and 13, and the viahole 11 are formed in a predetermined part. If it passes through the above process, the desired substrate 1 for electronic-parts loading will be completed. And if the bare chip C1 is carried on the substrate 1 for electronic-parts loading produced by doing in this way, the electronic component mount device M1 like drawing 1 can be obtained.

[0026]Now, in this example, the inner layer conductor layers 3, 4, and 9b and the outer layer conductor layer 9b which connect between the pads 12 and 13 are always wired a forward direction and centrifugal toward the substrate peripheral part, being connected by the viahole 11. Therefore, it differs from the conventional structure of pulling back again the wiring once pulled out to the peripheral part to a central direction (refer to drawing 3). Therefore, the length of the wiring which connects between the pads 12 and 13 becomes short, and wiring efficiency of a part without pull back of such wiring also improves certainly. For this reason, the electronic component mount device M1 with quick processing speed is realizable.

[0027]In this example, the adhesives for additives which become acid etc. from the heat resistant resin particle of fusibility at a poorly soluble photopolymer, acid, etc. are used in formation of the buildup layer B1 and the layer insulation layers 8a and 8b which constitute B-2. Therefore, it is hard to produce the development remainder on the bottom of the crevice for viahole formation at the time of exposure. Therefore, the viahole 11 of a byway can be formed easily and certainly conventionally. Of course, the conductor layers 9a and 9b formed by an additive process will become FAIN compared with what is formed in accordance with the conventional subtractive process. That is, the above composition is very convenient for the miniaturization of the substrate 1 for electronic-parts loading.

[0028]In this substrate 1 for electronic-parts loading, there is the feature that wiring is formed not only in the conductor layers 3 and 4 of the double-sided board 2 but in the buildup layer B1 and the conductor layers 9a and 9b of B-2. Even if the double-sided board 2 has the through hole 6, it does not have an adverse effect in particular on wiring, and it becomes unnecessary for this reason, to secure like before the space which can wire. This means that enlargement of the substrate 1 for electronic-parts loading is certainly avoidable.

[0029]And in this substrate 1 for electronic-parts loading, the buildup layer B1 of the almost same thickness as the surface S1 and the rear face S2 and B-2 are provided. For this reason, the size of the stress added to the both sides of the double-sided board 2 becomes almost equal, and stress becomes is easy to be offset mutually as a result. Therefore, the substrate 1 for electronic-parts loading which does not curve easily is realizable.

[0030] This invention can be changed as follows, for example.

(1) The electronic component mount device M2 which carries the bare chip C1 on the substrate 18 for electronic-parts loading of example of another is shown in drawing 2. With this substrate 18 for electronic-parts loading, it is the surface S1. The buildup layer B3 of the three-tiered structure is formed only in the side. On the other hand, the pad 13 which constitutes the 2nd pad group is the rear face S2. It is connected to the conductor layer 4 formed in the side. And rear face S2 On the whole, the rear conductor layer 4 is covered with the solder resist 19. Even if it is such composition, the same operation effect as an example is done so.

[0031] (2) The buildup layer B1 - the number of laminations of B3 (number of layers of the layer insulation layers 8a and 8b) may not be limited to two-layer or three layers, and may be four layers, five layers, six layers, seven layers, and eight layer -- one layer. Surface S1 The near number of laminations and the rear face S2 The near number of laminations may not necessarily be the same.

[0032] (3) As a base board, it may replace with the example which uses the double-sided board 2, and multilayer boards, such as 4 lamellae, 5 lamellae, 6 lamellae, 7 lamellae, and 8 lamellae, may be used. It is advantageous to choose the double-sided board 2 to give priority to low cost-ization, and it is advantageous to choose a multilayer board to attain further densification and miniaturization.

[0033] (4) It is possible to replace with the vamp 14 of an example and to form a pin etc. on the pad 13 which constitutes the 2nd contact button group. Of course, it is also possible to have composition which forms neither the vamp 14 nor a pin.

[0034] (5) The number of element-placement area may be one like an example, or it may be plural.

(6) The pad 13 which constitutes the 2nd pad group is the rear face S2. It may be provided over near whole buildup layer B-2. More pads 13 can be arranged as it is this composition.

[0035] (7) The conductor layers 9a and 9b which constitute the buildup layer B1 - B3 may be metal plating (for example, electroless nickel plating, unelectrolyzed gilding, etc.) other than non-electrolytic copper plating. It is also possible to choose the metal layer which replaces with the metal layer formed by a chemical method for film deposition like plating, for example, is formed by the physical thin film methods, such as sputtering.

[0036] (8) The electronic parts carried on the substrate 1 for electronic-parts loading may be semiconductor packages, such as PGA which has BGA, QFN, and a short pin other than the bare chip 2 of an example, for example.

[0037] (9) As [enumerate / besides the combination of an example / the combination (R1+R2+R3) of the resin which sensitization-ized thermosetting resin, thermoplastics, and heat resistant resin / below] that is, R1. + R2. + R3. = Epoxy acrylate + PES+ amino resin, Epoxy acrylate + PSF+EP, epoxy acrylate + phenoxy resin +EP, epoxy acrylate +PE+EP, epoxy acrylate +PSF+ amino resin, epoxy acrylate + phenoxy resin + amino resin, Epoxy acrylate +PE+ amino resin, epoxy acrylate +PES+ amino resin and EP, epoxy acrylate +PSF+ amino resin and EP, epoxy acrylate + phenoxy resin + amino resin and EP, epoxy acrylate +PE+ amino resin. And EP, photosensitive PI+PES+EP, photosensitive PI+PES+ amino resin, photosensitive PI+PSF+EP, photosensitive PI+ phenoxy resin +EP, photosensitive PI+PE+EP, photosensitive PI+PSF+ amino resin, photosensitive PI+ phenoxy resin + amino resin, Photosensitive PI+PE+ amino resin, photosensitive PI+PES+ amino resin and EP, photosensitive PI+PSF+ amino resin and EP, photosensitive PI+

phenoxy resin + amino resin and EP, photosensitive PI+PE+ amino resin and EP, epoxy acrylate. And photosensitive PI+PES+ amino resin, epoxy AKURI. A rate. And photosensitive PI+PSF+EP, epoxy acrylate. And photosensitive PI+ phenoxy resin +EP, epoxy acrylate and photosensitive PI+PE+EP, epoxy acrylate and photosensitive PI+PSF+ amino resin, epoxy acrylate and photosensitive PI+ phenoxy resin + amino resin, epoxy acrylate. And photosensitive PI+PE+ amino resin, epoxy acrylate. And photosensitive PI+PES+ amino resin and EP, epoxy acrylate, photosensitive PI+PSF+ amino resin and EP, epoxy acrylate, photosensitive PI+ phenoxy resin + amino resin and EP, epoxy acrylate, photosensitive PI+PE+ amino resin, and EP. Of course, even if it is a possible combination of others which were not enumerated here, it approves.

[0038]Here, the technical ideas grasped by the example and example of another which were mentioned above are enumerated below with the effect besides the technical idea indicated to the claim.

(1) In either of claims 1-3, said buildup layer should be provided in both sides of the base board. Wiring efficiency can be improved more as it is this composition, and it becomes difficult to produce curvature.

[0039](2) Said layer insulation layer should consist of the epoxy acrylate acrylic-ized 25%, PES, an epoxy resin particle (mixture (5.5 micrometers and 0.5 micrometer)), and a photosensitive monomer in claim 1. Wiring efficiency can be further improved as it is this composition.

[0040](3) The epoxy resin particle was replaced with melamine resin particles in the technical idea (2). Wiring efficiency can be further improved as it is this composition. The technical term used into this specification is defined as follows.

[0041]"acid or oxidizer : -- chromic acid, chromate salt, fault manganese salt, chloride, phosphoric acid, formic acid, sulfuric acid, fluoric acid, etc. which are used in surface roughening process are pointed out -- "

[0042]

[Effect of the Invention]As explained in full detail above, according to the invention according to claim 1 to 4, the substrate for electronic-parts loading which can raise wiring efficiency can be provided, avoiding the whole enlargement. In particular, according to the invention according to claim 2 to 4, the whole enlargement can be avoided more certainly.

[Brief Description of the Drawings]

[Drawing 1]The outline sectional view showing the substrate for electronic-parts loading of an example.

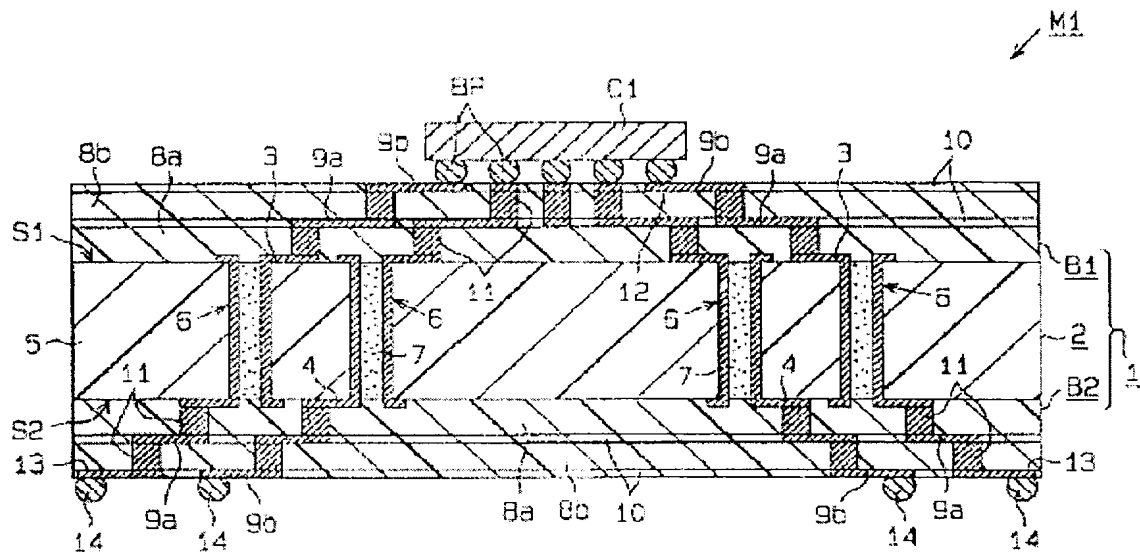
[Drawing 2]The outline sectional view showing the substrate for electronic-parts loading of example of another.

[Drawing 3]The outline sectional view showing the substrate for electronic-parts loading of a conventional example.

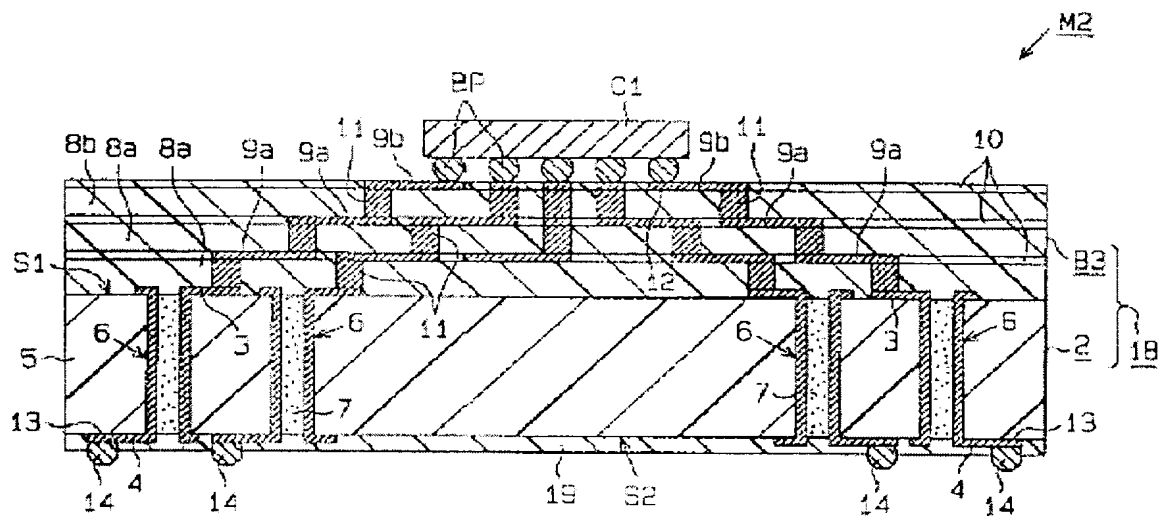
[Description of Notations]

1, 18 [-- A viahole, 12, 13 / -- The pad as a contact button, and S1 / -- The surface and S2 - A rear face B1 B-2, and B3 -- Buildup layer.] -- The substrate for electronic-parts loading, 8a, 8b -- A layer insulation layer, 9a -- An inner layer conductor layer, 11

【図1】



【図2】



【図3】

